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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,458	07/23/2003	Hung-Chih Liu	SISP0003USA	1457

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MERRIFIELD, VA 22116

EXAMINER	
JEANGLAUDE, JEAN BRUNER	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 04/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/604,458	LIU ET AL.	
	Examiner	Art Unit	
	Jean B Jeanglaude	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 8-11* is/are rejected.

7)☒ Claim(s) *4-11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07-23-03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objection

1. Claims 1, 4, 5are objected to because of the following informalities: it is suggested to substitute "amplifierinput", "amplifier output" in claim 1, lines 17, 20 respectively by – amplifier input --, -- amplifier output -- . It is suggested to substitute "anda" in claim 4, line 4 by – and a --. It is suggested to substitute "filterconnected" in claim 4, line 6 by – filter connected --. It is suggested to substitute "digitalbinary-valued—in claim 5, line 2 by – digital binary valued --. Appropriate correction is required.

Specification

2. It is suggested not to refer to the invention as "the claimed invention" throughout the specification, for instance in the summary of the invention, paragraphs 18 – 25.

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1 – 3, 8 - 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art (APA) in view of Choi et al. (US Patent Number 6,59,392).

6. Regarding claims 1 – 3, 8, 9, 10, the APA discloses a multiplying digital-to-analog converter (MDAC) stage in series (figs. 1 – 3) for a pipelined analog-to-digital converter (fig. 3 is a block diagram of one MDAC) , the MDAC stage comprising: an input node (V_j) for receiving an analog signal; a sub-analog-to-digital converter (the encoder 36, and the comparators 32, 34 in fig. 3 form the sub-analog-to-digital) for converting the analog signal to a digital code; an amplifier (44, fig. 3); a first capacitance (C_1) selectively connected between the input node (V_j) and the amplifier input and between the amplifier input and the amplifier output (fig. 3) wherein during a sample phase the first capacitance is connected between the input node and the amplifier input (fig. 3) and during a hold phase the first capacitance is connected between the amplifier input (fig. 3). The APA does not disclose a multiplying digital to analog convert stage for a pipelined ADC that comprises a plurality of second capacitances in parallel selectively connected between the input node and the amplifier input and between a corresponding plurality of digital reference signals and the amplifier input, the plurality of digital reference signals comprising digital signals corresponding to the digital code and a first calibration signal; wherein during a sample phase the first capacitance is connected between the input node and the amplifier input and the plurality of second capacitances are connected in parallel between the input node and the amplifier input, and during a hold phase the first capacitance is connected between the amplifier input and the

amplifier output and the plurality of second capacitances are connected in parallel between the plurality of digital reference signals and the amplifier input (claim 1) and a MDAC stage wherein the sum of the plurality of second capacitances is nominally equal to the first capacitance (claim 2). However, Choi et al., in a related field, discloses a multiplying digital to analog convert stage (figs. 1, 7) for a pipelined ADC that comprises first capacitance (C_0) and a plurality of second capacitances (C_1,...,C_8) in parallel selectively connected between the input node (Ai1) and the amplifier input (the input of the amplifier 220) and between a corresponding plurality of digital reference signals (V_{ref}) and the amplifier input (the input of the amplifier 220), the plurality of digital reference signals (V_{ref}) comprising digital signals corresponding to the digital code and a first calibration signal (figs. 1, 7; paragraph bridging col 5 an 6; col 6, lines 10 – 23); and the plurality of second capacitances are connected in parallel between the input node and the amplifier input (figs. 1, 7), and the amplifier output and the plurality of second capacitances are connected in parallel between the plurality of digital reference signals and the amplifier input (fig. 1, 7) and a MDAC stage wherein the sum of the plurality of second capacitances is nominally equal to the first capacitance (fig. 7; the capacitors are in parallel, the total capacitance of C1 to C8 is less or equal to C0). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the applicant's admitted prior art with that of Choi et al. in order to provide multiplying DACs and converting methods that can include capacitor errors.

7. Regarding claim 11, the combination of the APA and Choi et al. would achieve the same end result as a first and second calibration signals that are random digital

binary valued sequences having the same waveform (see fig. 4 of the APA and figs. 13A, 13B of Choi et al.).

Allowable Subject Matter

8. Claims 4 – 7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. Reasons for allowing claims 4 – 7 will be provided in the next office action.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

11. Lim et al. (US patent Number 5,635,937) discloses a pipelined multi-stage ADC.

12. McCarroll et al. (US patent Number 5,977,894) discloses a digital calibration for ADCs with implicit gain proration.

13. Hisano (US Patent Number 6,489,904) discloses a pipeline ADC with on chip digital calibration.

14. Aram (US patent Number 6,545,628) discloses an analog-to-digital converter with enhanced differential non-linearity.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jean B Jeanglaude whose telephone number is 571-272-1804. The examiner can normally be reached on Monday - Friday 7:30 A. M. - 5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jean Bruner Jeanglaude
April 09, 2004

JEAN JEANGLAUDE
PRIMARY EXAMINER